Load-Modulation Technique for Next Generation Mobile

Ahmed M. Abdulkahleq
Research and Development
SARAS Technology LTD
Leeds, UK
a.abd@sarastech.co.uk

Maan A. Yahya
Computer systems
Northern Technical University, Mosul, Iraq
dr.maan@ntu.edu.iq

Jack Brunning
Research and Development
SARAS Technology LTD
Leeds, UK
Jack.Brunning@sarastech.co.uk

Yasir Al-Yasir
School of Engineering and Informatics
University of Bradford
Bradford, UK
Y.I.A-Al-Yasir@bradford.ac.uk

Naser O. Parchin
School of Engineering and Informatics
University of Bradford
Bradford, UK
n.ojaroudiparchin@bradford.ac.uk

Ashwain Rayit
Research and Development
SARAS Technology LTD
Leeds, UK
ashwain.rayit@sarastech.co.uk

Raed A. Abd-Alhameed
School of Engineering and Informatics
University of Bradford
Bradford, UK
r.a.a.abd@bradford.ac.uk

James Noras
School of Engineering and Informatics
University of Bradford
Bradford, UK
J.M.Noras@bradford.ac.uk

Abstract—In this research, an asymmetrical load-modulation power amplifier is proposed and described. The designed amplifier uses two GaN HEMT transistors with 25W and 45W peak power. The designed amplifier is targeting the sub-6 GHz 5G spectrum with 200 MHz bandwidth at a center frequency of 3.4 GHz to achieve a 70 W peak power with peak efficiency at 8 dB back-off. The performance of the fabricated circuit was able to show good efficiency at the back-off region. In addition, the amplifier was tested using a continuous wave (CW) and an 8 dB peak-to-average power ratio (PAPR). The measurements results using CW reveal a power-added efficiency (PAE) of 45% at 40 dB average output power with a 31 dB adjacent channel power ratio. Good isolation between the amplifiers’ input is needed to minimize the effect of the reflected waves on the load-modulation operation.

Keywords— load modulation, quarter-wavelength, Doherty amplifier, back-off power, efficiency, AM/AM, AM/PM.

I. INTRODUCTION

The power amplifier is an essential component in any mobile communication system, where its primary function is to enlarge the input signal amplitude without any distortion (Ideally). However, the power amplifier has two operational regions which are the linear and the non-linear regions [1-3]. In addition, the power amplifier has two essential properties which are the linearity and the efficiency; these properties are inversely proportional, where high linearity with poor efficiency can be achieved in the linear region and the poor linearity with high efficiency would be achieved in the non-linear region. As the input signal uses a more complex modulation scheme to increase the data rate and utilize the available bandwidth effectively, the envelope signal will be bigger, in this case the peak-to-average power ratio (PAPR) will be increased and the amplifier operation region needs to be backed off to keep the linearity requirement for designed system; however, the efficiency of the power amplifier drops sharply at this region, [4-10]. To improve power amplifier efficiency, several techniques can be used. These techniques were introduced at the beginning of the last century and known as the Doherty technique (load modulation), Envelope tracking (ET), Linear amplification using Nonlinear Components (LINC), Envelope Elimination and Restoration (EER) and Chireix Out-phasing. The Doherty technique is the simplest way of achieving efficiency at the back-off; since no additional circuitry is required [5].

The use of GaN HEMT transistors has several advantages including small in size, low parasitic capacitance, good thermal conductivity, high transition frequency, high current density, and high breakdown voltage. However, its minor drawback is the complex biasing polarity for the gate and the drain sides. In addition, the transistor biasing should follow a sequence, where the gate side should be biased negatively first, whereas the drain side should be then biased positively after that[1].

The transistor design should include, biasing circuits and stability in addition to the input matching network and output matching network; the gain performance is mostly controlled by the input matching network. It has been found that the input matching side can depend only on the fundamental frequency matching, whereas higher harmonic matchings can be neglected because it has a very small effect at the input side. On the other hand, the output matching network is in charge of the output power performance and achievable efficiency. The matching of the output side can depend on the fundamental and second harmonics only, however, including other harmonics can improve the transistor performance in the cost of the circuit complexity [5].

In this paper, the asymmetrical load modulation amplifier design and implementation will be discussed, where the main operation principle including the design steps will be presented. In addition, the simulations and the measurements results will be presented.

II. LOAD MODULATION PRINCIPLE

The load-modulation principle relies on the load-line characteristics which are an important measurement that...
illustrates the behaviour of the transistor drain-source current versus the drain-source voltage for different gate-source voltages. An example of load-line behaviour is shown in Fig. 1. From this figure, the transistor needs to see an optimum load impedance, its value can be calculated according to equation (1):

\[ R_{\text{opt}} = \frac{V_{dd} - V_{knee}}{I_{\text{max}}/2} \]  

where
\( R_{\text{opt}} \): Optimum impedance
\( V_{dd} \): Drain voltage
\( V_{knee} \): Knee voltage

At the same time, the transistor can be saturated and produce maximum voltage swing at lower current if the impedance seen by the amplifier is increased, and this represents the main characteristic that the load modulation technique depends on.

The classical load modulation amplifier consists of a splitter for dividing the input signal between the amplifiers, where the bating condition is the difference between the amplifiers. A class AB is used of the main amplifier whereas the peaking amplifier is biased as a class C. A combination network is used for combining the output power of the two amplifiers in addition to performing the load modulation, as shown in Fig. 2. The input signal is split between the two amplifiers, after that, the output signals of both amplifiers will be recombined using the load modulation network; where two regions can represent the operation of the load modulation which are:

1) **Low power region**
At this region, only the main amplifier is working, because of the peaking amplifier state (OFF) due to the low input level and the biasing condition which keeps the peaking amplifier OFF. In this case, the peaking amplifier can be assumed as an open circuit. Moreover, the impedance seen by the main amplifier will be twice than the matched impedance due to the inversion characteristic of the quarter-wavelength transmission line as shown in the following equation:

\[ Z_{\text{out}} = \frac{Z_{\text{in}}}{2} \]  

where
\( Z_{\text{out}} \): The impedance at the output of the \( \frac{\lambda}{4} \) transmission line
\( Z_{\text{in}} \): The characteristic impedance of the \( \frac{\lambda}{4} \) transmission line

It can be noticed from equation (2), the impedance can be increased only when the \( \frac{\lambda}{4} \) characteristic impedance is higher than the impedance at the input side (see Fig. 2.). In this case and according to Fig. 1, the amplifier will be saturated due seeing higher impedance and the voltage will be full swing.

2) **Load modulation region**
At the beginning of the load modulation region, the peaking amplifier starts working and feeding current into the summing node because the input signal level is enough to turn it on, as illustrated in Fig. 3 (the shaded area). It can be seen that the peaking amplifier acts as an additional current source. So that, the contributed current of the peaking amplifier will modulate the impedance seen by the main amplifier as shown on the next two equations:

\[ Z_M = \frac{Z_{\text{in}}^2}{R_L \left( \frac{I_{\text{in}}+I_p}{I_p} \right)} \]  

\[ Z_p = R_L \left( \frac{I_{\text{in}}+I_p}{I_p} \right) \]
It can be noticed from the equations above and by assuming that $R_i = Z_o/2$, there will be a change in the impedance seen by the main amplifier from $2Z_o$ to $Z_o$ depending on the value of the peaking amplifier current, whereas the change of the impedance seen by the peaking amplifier will be from infinity to $Z_o$. In addition, the power ratio between the two amplifiers plays an important role in determining the maximum achievable power and the back-off power region. The maximum peak power of the load-modulation amplifier will be the sum of peak power of both amplifiers, whereas the following equation can be used for calculating the output back-off power:

$$BP = 20\log\left(\frac{P_{\text{main}}}{P_{\text{main}} + P_{\text{peaking}}}\right) \quad (5)$$

where

- $BP$: Back-off Power
- $P_{\text{peaking}}$: peaking power in watt
- $P_{\text{main}}$: main power in watt

It can be noticed that for 25W and 45W the maximum achievable back-off power will be -8.9 dB from the peak power.

### III. DESIGN AMPLIFIER APPROACH

Practical power amplifier design has several steps that are needed to produce a certain amount of performance. The amplifier design starts by having all the required specifications which have an impact on selecting the transistor technology, power, and topology. After choosing the transistor, the verification of the scattering parameters and the model file of the device should be done because the whole design simulation depends on these files. Then, the transistor stability should be tested to make sure that no oscillation can occur, the amplifier design can be divided into three sub-circuits for simplicity, the transistor, at the input side, should be matched to an impedance so that a certain amount of gain and gain flatness over the required frequency band can be obtained. On the other side, the load-pull examination test including the fundamental and the harmonics can be done at the output side of the transistor to choose an impedance which represents a trade-off between the required amount of efficiency and output power. Both input and output matching sides should include the biasing network, which represents the dc feeding port, at the same time, it should block the RF signal from going towards the dc source.

After completing the matching network design for both amplifiers and according to the load modulation structure, the input signal needs to be split between the two amplifiers, where a Wilkinson power divider is designed for that purpose; the split ratio between the two amplifiers plays an important role for completing the load modulation between the amplifiers. Since the peaking amplifier is biased as class C, the maximum current of this biased class is lower than class AB amplifier, so that, Wilkinson divider can be designed to provide the peaking amplifier with more power than the main amplifier. In this case, the instantaneous gain of the main amplifier will be reduced because the input signal will be less. In addition, the isolation between the input of the two amplifiers should be good enough to prevent the reflected wave from affecting the load-modulation operation. On the output side, the load-modulation combiner consists of two quarter-wavelength transmission lines; the first one works as impedance inverter whereas the second one will be used as a global matching network. In order to complete the load-modulation design, there is a need for adding offset lines for each amplifier:

1. The offset line at the output side of the main amplifier will be used to compensate for the parasitic effect of the main amplifier.
2. On the other hand, the peaking amplifier needs an offset line at the output side to reduce the current leakage from the main amplifier towards the peaking amplifier.
3. Finally, due to the difference in biasing condition, an offset line at the input of the peaking amplifier is needed for compensating the phase difference between the amplifiers, plus a $\lambda/4$ transmission line to compensate the phase difference produced by the inverter at the output side.

### IV. SIMULATION AND PRACTICAL MEASUREMENTS

The fabricated circuit is shown in Fig.4 where the designed circuit was simulated using Microwave Office (MWO). The asymmetrical load-modulation amplifier is based on GaN HEMT technology using two transistors with different power capability, the main amplifier depends on CGH40025 to provide 25W whereas the peaking amplifier depends on CGH40045 to generate a peak power of 45W, so that that total achievable power using load-modulation architecture would be 70W, the output matching networks of both amplifiers are connected to each other using the quarter wavelength transmission line to compensate the phase difference produced by the inverter at the output side.

![Fig. 3. Ideal Current and voltage profiles for load-modulation amplifier](image-url)
The large signal measurements of the main and the peaking amplifiers working alone are shown in Fig.6 and Fig.7. It can be noticed that the small signal gain of the main amplifier is 13 dB and the peak power added efficiency is 63%. On the other hand, the large signal measurement for the peaking amplifier was tested when the peaking amplifier was biased as class AB, the small signal gain was 13 dB and the peak power-added efficiency was 65%. After checking the performance of the designed amplifiers, the load-modulation amplifier will be checked by keeping the biasing of the main amplifier and changing the peaking amplifier biasing to class-C by changing the gate-source voltage of the peaking amplifier to (-5.2V). the performance of the designed load-modulation amplifier is shown in Fig.8, it can be noticed that there is an efficiency peak of 45% at the output back-off power of 8dB from the peak power. The fabricated asymmetrical load-modulation amplifier was tested with a modulated signal of 8 dB PAPR when the average output power was 40 dBm and the achieved power added efficiency was 44% and the Adjacent channel power ratio (ACPR) was 31 dB which can be improved using a Digital pre distorter (DPD).

Besides, the impedance seen by both amplifiers was tested as shown in Fig.9, it is clear that the impedance seen by the peaking amplifier before the back-off region is too high whereas the impedance seen the main amplifier at the same region is about 110Ω. However, in the load-modulation region, the impedance seen by both amplifiers will be modulated and reduced to 50Ω at the peak input power, where both amplifiers give their maximum designed power.

On the other hand, the Amplitude-to-Amplitude (AM-AM) and Amplitude-to-phase (AM-PM) is illustrated in Fig.10, where it can be noticed that good linearity has been achieved using this technique.
Moreover, the voltage and current profiles of the load-modulation amplifier are illustrated in Fig. 11 and Fig. 12. It is obvious that the main amplifier will provide almost full voltage swing at the back-off, whereas, the peaking amplifier will start injecting current.

V. CONCLUSIONS

The design principle of load modulation power amplifier is discussed, where 70W asymmetrical load-modulation amplifier using two GaN HEMT devices were designed, fabricated and tested. The peaking amplifier biasing deepness affects the maximum current provided by the peaking amplifier and will affect the load modulation operation. In addition, the isolation between both amplifiers at the input side is so important to prevent the effect of the reflected waves on the load-modulation operation. The first peaking efficiency is a result of saturating the main amplifier, so that, the back-off efficiency is mainly controlled by the main amplifier if the peaking amplifier leakages are ignored. The fabricated circuit was tested with CW and a modulated signal of 8-dB PAPR at 40 dB average power, good linearity of 31 dB was achieved which can be corrected by a DPD. The offset lines play an important role in compensating the phase difference between both amplifiers, in addition to reducing the current leakage from the main amplifier towards the peaking amplifier.

ACKNOWLEDGMENT

This research has received support from the European Union’s Horizon 2020 research and innovation programme under grant agreement H2020-MSCA-ITN-2016 SECRET-722424. [11]


