Advancement of a Highly Efficient Class-F power Amplifier for 5G Doherty Architectures

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Abstract—This paper presents a saturated Doherty power amplifier based on Class-F topology using unmatched GaN HEMT transistors for its high efficiency, high gain, and wide bandwidth capabilities. The Design topology of high efficiency switch-mode Class-F by controlling second and third harmonics and its linearity performance are studied, which ensures an improvement in Doherty operation at 3.6 GHz frequency band for 5G applications. The simulation results prove that the realized DPA achieves a peak power added efficiency of 55% at 43.58dBm output power, which improved by 10% in contrast to the conventional class AB/C Doherty.

Keywords—High power amplifiers; high efficiency; Doherty power amplifier, Class F power amplifier 4G, 5G, GaN-HEMT.

I. INTRODUCTION

The evaluation of 5G mobile telecommunication services has been targeting expanded carrier aggregation and advanced use-cases to enable high speed connectivity [1]. An RF Power Amplifier (PA) has a fast evolving and expansive topic that consistently molded to fit new system requirements. The Doherty Power Amplifier (DPA) is one of the strong candidates among efficiency enhancement approaches for 5G wireless communication systems because of its wide aggregated instantaneous bandwidth and tunable efficiency characteristics [2]. A variety of advanced DPA design techniques have been adopted, including the uneven power drive, gate bias adoption, harmonic tuning strategies and digital Doherty using digital signal processing for phase synchronization. However, usually increases the circuit complexity and requires additional cost to implement [3,4]. Among advanced DPA techniques, the so-called saturated Doherty scheme has drawn the most attention because of its capability of outputting high power and delivering high PAE performance [5]. In fact, the harmonic generating mechanism enables the Doherty PA to operate at quite high frequency (up to the X-band) for smart manufacturing applications. A number of practical aspects related to the finite number of harmonics, which may be efficiently controlled in actual devices are addressed in [6-7]. In [8] the authors propose a new asymmetric Class-F’ F GaN Doherty using Fourier transforms to compensate the low output current of peaking device. As a result, an improper load modulation is effectively modified. In other work [9] a blended Class-EF mode and load-pull technique for fundamental-frequency are proposed. The fabricated DPA delivers acceptable peak output power of 40.4-dBm at 84.4% drain efficiency. In addition, to overcome the nonlinearity issue associated with Class-F DPA, due to operating in saturation mode, many linearization techniques have been adapted to variable envelope systems [10-11].

This contribution, addresses the opportunity to evaluate the performance of high efficiency Class-F PA by focusing on figure of merit characteristic of power amplifier and develop the conventional Doherty configuration with the Class-F waveforms transformation. Dissimilar fundamental current, driving between carrier and peaking amplifiers as a function of input power can improve the active load modulation operation.

The work is organized in the following sections. Section II will analysis the Class-F output power and efficiency up to the 3rd harmonic components. Also, the design topology of Class-F PA using load-pull technique has been presented in this section. Section III will discussed design procedure of Doherty PA incorporating Class-F PA in carrier and peaking stages and the ADS simulation results will be compared with that of conventional DPA. Some conclusion will be discussed at the end in section IV.

II. CLASS-F OUTPUT POWER AND EFFICIENCIES

A. Circuit topology

Highly efficient operation of power amplifier can be obtained by polyharmonic modes of widely accepted Class-F amplifier, when an additional multi-resonant circuit terminates the device output with short-circuited of even harmonic frequencies and open-circuited of odd harmonics [12]. Class-F PA controls the waveforms at the device output to achieve the maximum efficiency and reduces the overlapping area between voltage and current waveforms by reducing the transition time of two signals, which leads to decreasing the dissipated power. The second and third harmonic voltage components have the main contribution on Class-F design and higher order imply impractical suggestion because of circuit complexity. Therefore, in this work, the voltage waveform is expressed by DC, fundamental and third harmonics components combination. The DC power consumption and Output power can be computed by the following equations, where, the waveform is depending on the DC bias and the input drive level expanded in the Fourier series up to the 3rd harmonic components;

\[ P_{DC} = \frac{\max V_{DC}}{2\pi} \cdot \frac{2 \sin(a/2) - a \cos(a/2)}{1 - \cos(a/2)} \]  \hspace{1cm} (1)
where $I_{\text{max}}$ is the maximum drain current and $\alpha$ is the drain current conduction angle that depends on the DC current.

\[
\alpha = 2 \cos^{-1}\left(\frac{I_{\text{DC}}}{I_{\text{DC}} - I_{\text{max}}}\right) \tag{2}
\]

\[
P_{RF} = \frac{I_{\text{max}}/2 + V_{\text{DC}}}{2\pi} \left(\alpha - \sin \alpha \right) \cdot \gamma(\varepsilon_3) \tag{3}
\]

\[
\gamma(\varepsilon_3) = \left(\frac{V_{f_0} - V_{DC}}{V(t) - V_{DC}}\right) \tag{4}
\]

\[
\varepsilon_3 = \left[ \cos \omega_0 t + \frac{R_L f_0 f_3}{R_L f_0 f_3} \cos 3\omega_0 t \right]^{-1} \tag{5}
\]

The gain coefficient $\gamma(\varepsilon_3)$ can be defined as the ratio between fundamental and third-harmonic drain voltage waveform, where the Class F drain voltage consists of the DC, fundamental, and third-harmonic components:

\[
V(t) = V_{DC} - V_{f_0} \cos(\omega_0 t) - V_{f_3} \cos(3\omega_0 t) \tag{6}
\]

Higher output power can be obtained by greater fundamental voltage and unaffected dissipated power by third harmonics. Thus, the improved drain efficiency can be expressed by:

\[
\eta = \frac{1}{2} \left(1 - \frac{V_k}{V_{DC}}\right) \cdot \frac{\alpha - \sin \alpha}{2 \sin(\alpha/2) - \alpha \cos(\alpha/2)} \cdot \gamma(\varepsilon_3) \tag{7}
\]

Where $V_k/V_{DC}$ is the normalized knee voltage. It can be noticed that the output power and drain efficiency will be enhanced by the gain coefficient.

**B. Design consideration**

Class F amplifier is mostly biased at pinch-off, where all the odd harmonics of a half-sinusoidal current waveform are nullled, however, conduction angles other than 180° commonly are the reason of creating all harmonics. Consequently, the flatness of Class-F voltage waveform during the period of conduction should be shaped by adding the single harmonic [13]. In order to achieve the optimum load impedances that compromise the power added efficiency and output power contours, the load-pull simulation is performed on a nonlinear model of Cree’s 10-W CGH40010F GaN HEMT device with a high gain at the 3.6 GHz center frequency. HEMT device is chosen for providing wide bandgap and high thermal conductivity for a high power operation [14]. The gate and drain bias voltages are set to $V_{GG} = -3.1$ V and $V_{DD} = 28$ V. In this work, Rogers4350B substrate with dielectric constant $\varepsilon_r = 3.66$ and thickness $h = 0.762$ mm is applied.

Class-F PA design has been accepted to consider both input-output harmonics tuning using the wave shaping network for voltage and current waveform which, can be realized by means of microstrip transmission lines. The output network is tuned to resonance at the fundamental, second and third frequencies and the quarter-wave transformer, transforms the 50 ohm load to $R_L$ at the drain, which is determined to deliver the maximum excursions of drain voltage and current. The drain current contains only the even harmonics, while the drain voltages includes the odd harmonics. The input network provides a conjugate match at the gate input.

The load network that applied for Class-F along with the sub-matching network is depicted in Fig 1. It has series microstrip lines and microstrip stubs for harmonic control and fundamental matching and provides an open circuit condition at the third harmonic through TL1 and TL2 lines while, the combination of TL1, TL2 lines with TL4 presents short circuit condition at second harmonic. The stub of TL7 delivers perfect sinusoidal shape and improves the output voltage waveform. In fact, the number of harmonics determines the maximum attainable efficiency[14]. The sub-matching network at fundamental frequency is performed by $\pi$-shape transmission lines. Fig.2 indicates the input matching network of Class-F including a quarter wavelength and stubs to form the low pass filters whose purpose is to stop the delivery of harmonics power to the load. The $\lambda/4$ TL10 line provides a high impedance at third harmonic and a very low impedance at second harmonic component of the input signal. The resistors ensure the stability condition of amplifier and blocking capacitors are used in both sides to block DC components in the incoming and outgoing signals and permit the propagation of RF signals.

\[
\begin{align*}
\text{(a)} & \quad \text{(b)} \\
\text{Fig. 1. Schematic of the output harmonic circuit.} & \quad \text{Fig. 2. Schematic of the input harmonic circuit.}
\end{align*}
\]

The simulation results of gain flatness, drain efficiency, PAE and output power are presented versus input power in Fig.3(a, b). A maximum drain efficiency of approximately
70% has been achieved at 41.23dBm output power with 9dB gain flatness. The amplifier shows 52.50% PAE at input power of 33dBm. The optimum performance of amplifier at operating frequency of 3.6 GHz validates that by optimizing the PAE, Class-F PA, minimizes the power dissipated by the transistor under large signal operation. However, the maximum efficiency is specified only at maximum power and at 6dB back-off output power Class-F exhibits an efficiency of 35%, whereas, average efficiency may be the most important measure in determining the battery requirements for the transmitter.

Fig 4. Fourier voltage and current voltage waveforms with three harmonics. (a) Drain voltage (b) Drain current.

The drain current and voltage waveform are displayed in Fig. 4(a, b), respectively. The first and second harmonics current waveform are in phase to shape the drain current similar to a half-sinusoidal waveform, as can be seen in Fig. 4(a). A portion of it goes below zero, because of parasitic capacitance of transistor. The first and third harmonic voltage waveforms are out of phase to create the drain voltage waveform close to rectangular waveform in Fig. 4(b).

Fig 5. Input/output current waveforms with harmonics.

The appropriate ratio between amplitude of fundamental and third harmonic components may deliver the current waveform with huge difference between its fundamental and peak amplitudes as shown in Fig. 5. The in-phase combination of fundamental and second harmonic flattens the current waveform at the maximum values of voltage waveform and sharpens it at the minimum values of voltage waveforms. Thus, the integration across the period results in a reduction of power loss in contrast to the power that delivered to the load, when the maximum current corresponds to minimum voltage.

Fig 6. (a) AM/PM and (b) AM/AM characteristics without linearization.

Fig 7. Harmonic spectrum of Class-F at 3.6GHz

III. DOHERTY AMPLIFIER WITH CLASS-F CIRCUIT

The conventional two-way AB/C Doherty PA has a symmetrical structure based on the carrier amplifier and bias point of peaking amplifier. Both of active devices operate at the same drain voltage with equal matching networks, so that the length of compensation line is optimized to achieve an accurate active load modulation. However, the DPA is affected by some back-off efficiency issues attributed to the large power ratio between carrier and peaking amplifiers, due to different bias condition, that result in a non-optimal load modulation behavior.

In order to restore the proper load modulation, Doherty can employ the switching Class-F mode for tuning two main harmonic components that enable amplifier to provide higher efficiency and output power. Fig 8 presents the schematic of Class-F DPA, where the wave-shaping network includes the harmonic control parts and the fundamental matching network.

Fig 8. Schematic of Class-F based DPA.

When the peaking amplifier is turn-off at the back-off region, the carrier amplifier by terminating twice of the optimum load, maximizes the power added efficiency. Then, by increasing the input power above the peaking PA’s turn-on...
voltage, the carrier device gets into saturation and draws a “L” curve load line as can be seen in Fig. 9 (a), which results in the square-wave voltage and half-sinusoidal current signals. At the high power levels, both carrier and peaking PAs experience a reduction in the load impedances thus, their load lines rise up while maintaining the “L” shape. Due to the optimal load modulation of Class-F DPA, the peaking amplifier’s voltage and current swing are enlarged and reach the maximum sinusoidal current and square-wave voltage waveform at maximum power. Consequently, at peak power, peaking PA represents the same load line as carrier PA as shown in Fig. 9 (b). In fact, the peaking amplifier goes to saturation region only at maximum power.

Fig. 9. Load line of carrier and peaking PAs at different power levels

The simulation results of PAE, drain efficiency and gain against input and output power are presented in Fig. 10 (a, b). At 3.6 GHz the saturated Doherty amplifier provides a PAE of 55% at peak and 48% at 8dB OBO. It delivers the maximum drain efficiency of 65% at input power of 35dBm and enters saturation after an output power of 43.58dBm is achieved. A small signal transducer gain is flat at around 13dB when the amplifiers saturated, the gain decreases with increasing the output power.

The conventional Doherty simulation results in Fig. 11 (a, b), show the worse gain flatness than that of Class-F Doherty due to the class C bias condition of the peaking transistor, which is flat at around 12dB. The PAE of DPA at the 6dB back-off and maximum output power of 44.15dBm point reaches 50%.

Fig. 10. Efficiency and gain characteristic of Class-F Doherty PA.

Fig. 11. Efficiency and gain characteristic of conventional B/C Doherty PA.

Table 1 shows the performance comparison of current reported Class-F/F−1 DPAs. It confirms that the presented DPA, offers reasonable efficiency at 8dB back-off level.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Freq. (GHz)</th>
<th>Architecture</th>
<th>Gain(dB)</th>
<th>Pout(dBm)</th>
<th>Drain Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15]</td>
<td>2.4</td>
<td>2-way symmetrical</td>
<td>13.9</td>
<td>45.3</td>
<td>69.7</td>
</tr>
<tr>
<td>[16]</td>
<td>2.14</td>
<td>2-way asymmetric</td>
<td>10.6</td>
<td>43.1</td>
<td>57</td>
</tr>
<tr>
<td>[17]</td>
<td>3.45</td>
<td>2-way symmetrical</td>
<td>10</td>
<td>40 at 6dB OBO</td>
<td>52</td>
</tr>
<tr>
<td>[18]</td>
<td>2.14</td>
<td>4-stage symmetrical</td>
<td>10</td>
<td>43</td>
<td>61</td>
</tr>
<tr>
<td>This work</td>
<td>3.6</td>
<td>2-way symmetrical</td>
<td>13</td>
<td>43.58</td>
<td>65</td>
</tr>
</tbody>
</table>

IV. CONCLUSION

This article reviews the harmonic controlled class-F operation and presents the highly efficient saturated Doherty amplifier using a GaN HEMT transistor for 3.6 GHz frequency. The crucial role of the load impedance at the signal harmonics on power added efficiency and output power enhancement have been evidenced. It can be concluded that efficient DPA can be obtained through optimum load impedance terminations at the fundamental frequency, second and third harmonics, which can compensate the low current drive of peaking device in conventional DPA. The presented Class-F DPA module shows its potential to employ in 5G mobile communication relies on C-band spectrum, since it is able to achieve a high efficiency and high output power.

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